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# Efficient modelling of a modular multilevel converter

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**Abstract**—Looking at the near future, we see that offshore wind penetration into the electrical grid will continue increasing rapidly. Until very recently, the trend has been to place the offshore wind farms close to shore within the reach for transmission using HVAC cables but for larger distances HVDC solutions need to be considered. In the present work are presented methods to simulate the converter without using any kind of semiconductors in order to reduce the simulation time. The model consists only of passive components representing the sub modules in different states. For each state, new values are calculated for the converter. Time-domain simulations on a MMC HVDC test system are performed in the PSCAD/EMTDC software environment based on the new model. The results demonstrate that the modeled MMC-HVDC system with or without converter transformer is able to operate under specific fault conditions.

**Index Terms**-- *Modular multilevel converter, High frequency modeling, High voltage direct current (HVDC) transmission, Electromagnetic transients (EMT) simulation,*

## I. INTRODUCTION

In recent years there has been an increasing development and deployment of renewable energy sources to meet the new limitations of fossil fuels as an energy resource. This has given a large growth in the establishment of offshore wind farms. The increasing trend of offshore wind energy has meant that, in order to harvest the best wind conditions, larger distances from shore is needed [1]. Increased distance to shore means that the connection between farm and the onshore grid connection point by means of traditional AC-transmission lines becomes proportionally more infeasible. This is due to the limitations of long AC- cables, such as high resistive losses in the cables, the capacitive current and inductances causing problems with voltage stability. HVDC-based transmission technologies therefore are getting attractive as an alternative wind power transmission system [2]. Furthermore, HVDC-technology is used to non-synchronous grids, and hence HVDC-technology is expected to form the backbone of the future super grids. One of the important aspects to be considered in connection with HVDC transmission systems is the transient behaviour, including both components that are able to generate steep flanks all around the power system and the transients that can occur in fault situations. For transient investigations in all kinds of power systems, usually high frequency models are necessary and for HVDC, this includes the converters, and, in

particular regarding future systems, the more flexible voltage source converters (VSC). Due to the VSC's ability to connect large offshore wind power plants to the onshore grid, and furthermore its ability of connecting asynchronous networks, while keeping the stability of the power system, it offers the opportunity for considerable integration of a larger share of renewable energy in the power system.

In the present paper will be presented a VSC-model based on passive components, suitable for numerical simulations in time domain. Even though VSC is a well-known topology, only few modelling approaches seem to be available, especially regarding transients and the related high frequency range. A possible reason for this might be the large number semiconductor switches in a modular multilevel converter (MMC). Simulating such complex components with a considerable number of nodes in electromagnetic transient simulation programs such as PSCAD will have a negative effect on the calculation with simulation times being remarkably increased, often up to non-acceptable levels. In the present work are presented methods to simulate the converter without using any kind of semiconductors in order to reduce the simulation time. The model consists only of passive components representing the sub modules in different states. For each state, new values are calculated for the converter. In order to cover the transient and high frequent range, all parasitic components, in in this case mainly of capacitive character had to be added to the model. All contributions are taken into account forming a mathematically and dynamically equivalent, which models the entire converter. That accurate and well defined model allows for a considerable reduction of the simulation time. Time domain simulations of a back-to-back VSC demonstrate the capabilities of the model.

## II. MODULAR MULTILEVEL CONVERTER

MMC converters are built up of a large number of identical, but individually controllable submodules. The topology of the submodules in the MMC can vary according to the specific purpose of the construction. They can be built as a two-level half bridge topology with the capability of producing  $V_{SM}$  and zero. The second choice could be a two-level full bridge construction with the ability to produce  $\pm V_{SM}$  and zero. This is what makes the MMC special compared with other converter topologies the ability to control the submodules as a voltage source with a discrete number of voltage steps. Due to this behavior, the  $du/dt$  has been reduced significantly, resulting in a momentous reduction of the harmonics, which

reduces the need for filters or additional transformer and cable insulation.

As it is seen from figure 1, the modular multilevel converter is made of three phase legs/units, one for each phase. Each phase unit consists of an upper and a lower arm, connected in series between the dc terminals. The ac terminal is placed at the midpoint of the two arms. The phase arm consists of an inductor and a number of  $N$  series connected half-bridges with dc capacitors, also called submodules.

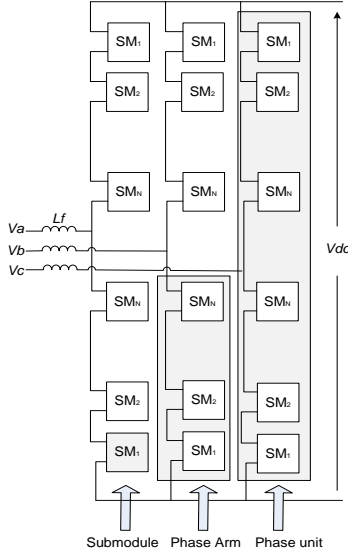


Figure 1: The structure of the MMC with 3 phase legs. The gray areas show a submodule, a phase arm and a phase unit.

As it is seen from figure 1, the main component of the modular multilevel converter is the submodule. The half-bridge submodule consists of two valves and a capacitor in parallel. Each valve consists of an IGBT with a freewheeling diode located in anti-parallel, see figure 2. Only one of the valves is switched on at any given time, and depending on the current direction, the capacitor will be charged or discharged [3]. When one of the valves is turned on, either the IGBT or the freewheeling diode is conducting depending on the current direction. The submodule can attain two different states, being either turned on or turned off [4].

#### State 1 – turned on

The definition of the submodule being turned on means that the IGBT T1 in the figure 2 below is conducting while T2 is off, which means that the current is being conducted through the submodule capacitor. If the multivalve current  $I_{sub}$  is positive, it will get charged, otherwise discharged. Meanwhile the voltage across T2, which is turned off, will be the same as the voltage across the submodule capacitor.

#### State 2 – turned off

When the submodule is turned off, T2 is conducting and T1 has stopped conducting. Therefore the current will be bypassing the submodule capacitor and the submodule will be seen as a short circuit. As a result of this, the voltage across

T2 will be 0 and the submodule capacitor will maintain the existing charge.

A third state, normally not used under operation, is that both valves are off and the current are conducting through the freewheeling diodes. Under these circumstances the direction of the current decides if the capacitor is charged or not.

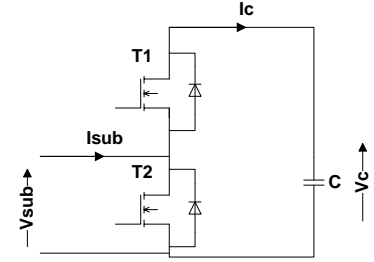


Figure 2: Main component of MMC the submodule.

The blocking voltage in each phase of the MMC should be twice the dc voltage  $V_{dc}$ . Due to the situation where all submodules in a phase multivalve are bypassed which will give a voltage that is equal to the dc voltage. The lower multivalve has to be able to block the entire dc voltage.

In a converter applying the MMC-topology, the number of steps of the output voltage is related to the number of series connected submodules and their state, if they are turned on or off. Each phase arm of the MMC consists of a stack which together forms a valve. There are two valves for each phase (e.g. upper and lower). The submodule capacitors are nominally charged to a desired voltage. This means that the output voltage is dependent on the number submodules turned on in each arm. Since the capacitor voltages of each submodule will add up to the net output voltage, this voltage can be determined from the expressions (1) and (2) below.

The output voltage of the converter, based upon the number each of submodules turned on in the lower arm is [5]:

$$V_{lower} = V_0 + \frac{V_{dc}}{2} \quad (1)$$

The output voltage of the converter, based upon the number of submodules turned on in upper arm is [5]:

$$V_{upper} = -V_0 + \frac{V_{dc}}{2} \quad (2)$$

Where  $V_{lower}$ , the combined voltage of the submodules, is turned on in the lower arm and  $V_{upper}$  is the combined voltage of the submodules turned on in the upper arm. The sum of the voltage in lower and upper arms should always be half the dc voltage in order to get zero dc offset at the phase output. The sum of the on-submodule voltages is kept constant, since inserting a submodule in the upper multivalve means bypassing on in the lower multivalve.

Figure 3 gives a graphical explanation of the operation of the MMC under two different situations. In the figure on the right, all submodules in the upper arm are turned on; hence the output voltage will be equal to the voltage of the negative

pole of the HVDC-system [6]. The figure on the left shows the opposite situation, in which all of the submodules in the lower arm are turned on, and hence the output voltage will be equal to the voltage of the positive pole [6]. From expressions (1) and (2) it is also clear, that when all the submodules in either the upper or lower arm are turned on, these submodules will actually be carrying the entire DC-voltage. This is due to the bipolar nature of the HVDC-system.

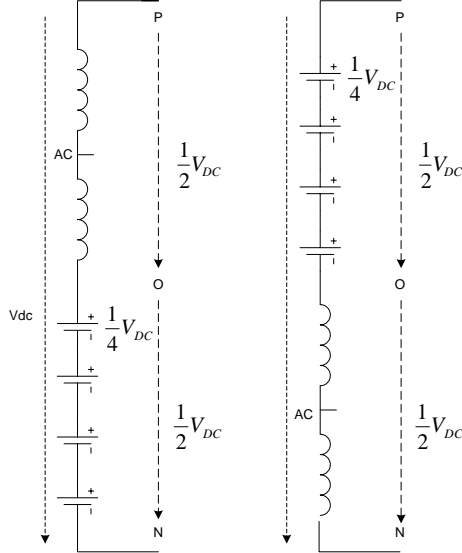


Figure 3: Operation of MMC single-phase diagram, Left: all lower submodule off and all upper submodule on Right: all lower submodule on and all upper submodule off.

The three phase legs of the converter impress the same DC voltage  $V_{dc}$ . And due to the fact that the converter is actually symmetrical, all three phase legs have the same impedance with respect to the dc terminals since they have the same number total of submodules in each leg. Knowing this, we recognize that the dc terminal current  $I_{dc}$  is split up among the three phase legs equally. In addition, each phase terminal current  $i_a$ ,  $i_b$  and  $i_c$  will also split up equally due to the fact that the converter is symmetrical.

### III. COMPONENT MODELING

When trying to model the IGBT in terms of passive components, we again have two situations. The first case is that IGBT is turned off, thus no current is flowing through it, which means that the IGBT will constitute a capacitance only [4]. However as there inevitably will be some inductance in the IGBT, this will have to be modeled as well by insertion of the inductor. Therefore the representation of the turned off IGBT will constitute in a capacitance in series with an inductor.

In case the IGBT is turned on, there will be some conductive losses, and these losses will represent the dynamic resistance of the IGBT [7]. Furthermore the inductance of the IGBT will have influence in high frequencies and needs to be included. Also, as it can be seen in figure 4, a capacitor has been placed in parallel, which is applied in order represent the capacitance of the IGBT. When the IGBT is turned on, a small forward

voltage exists across the IGBT due to its dynamic resistance, and when examining the voltage characteristics of the IGBT-capacitance it is clear that the capacitance of the IGBT is significant at low voltages.

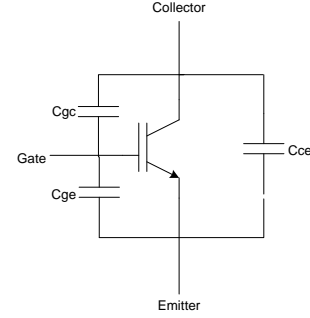


Figure 4: Capacitances of an IGBT [7]

In the datasheet of an IGBT, usually a number of capacitances are listed. Figure 4 shows 3 different capacitances in an IGBT, with a capacitance between each terminal of the IGBT. For this work we are not considering the optimization of the gate control in addition the sizes  $C_{ge}$  and  $C_{gc}$  in series are negligible compared with  $C_{ce}$  it doesn't contribute to our work to represent them individually, these 3 capacitances have been combined into a single capacitance.

#### A. Submodule Capacitor

For transient investigations, the submodule capacitor cannot simply be modeled as an ideal capacitor, as this component besides the capacitance also includes some inductance known as the Equivalent Series Inductance [ESL], which is mainly caused by the leads and internal connections used to connect the plates or foil to the outside environment. It is obvious that the ESL will get increased influence at high frequencies, in particular when approaching the resonance frequency formed together with the capacitor. The resistance known as the Equivalent Series Resistance [ESR] covers the physical series resistance in the physical capacitor (e.g. the ohmic resistance of the leads and plates or foils). Including all parasitic components, the model of the submodule capacitor looks as seen in the figure 5 [8].

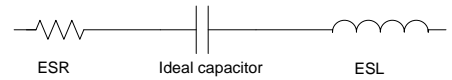


Figure 5: Equivalent circuit of the physical submodule capacitor. ESR: Equivalent Series Resistance, ESL: Equivalent Series Inductance

Due to the way, we have chosen to model the MMC and the lack of possibilities to choose start voltages and currents an vary the voltage across the capacitors in the simulation tool, the voltage change across the capacitor has to be calculated mathematically for each time step using equation (3).

$$V_c(t) = \frac{1}{C} \int_{t_0}^t I(t) dt + V_c(t_0) \Rightarrow \frac{I(t)}{C} \cdot \Delta T + V_c(t_0) \quad (3)$$

Here  $V_c(t)$  is the initial voltage across the capacitor,  $I(t)$  is the current through the component and  $\Delta T$  is the simulation time step. This integration will include the voltage changes in the submodule capacitors for each time step and thereby alter the total multivalve voltage.

### B. Submodule

In figure 6 the circuit diagram as implemented in PSCAD is shown for the situation in which the submodule is turned on. Here we have also added the protective thyristor as a capacitor for a more uniform picture of the submodule.

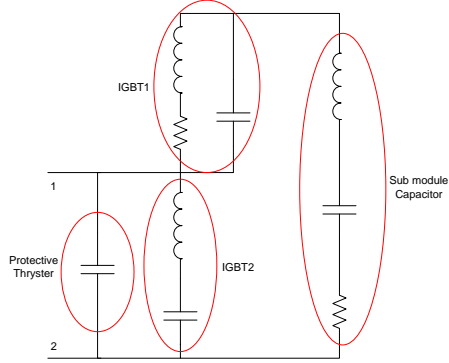


Figure 6: Principle submodule circuit in on-state as implemented in PSCAD

In figure 7 the circuit diagram is shown for the situation in which the submodule is turned off.

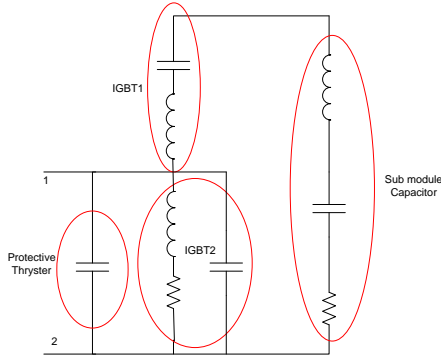


Figure 7: Principle submodule circuit in off-state, as implemented in PSCAD

From the figures above it can be seen, how a submodule is expressed in terms of passive components. Knowing that there are a number of  $N$  submodules connected in series, it makes the task of expressing them a bit more simple. All components are added together into two modules, representing all submodules, which are on and one for those which are off, this is done for each multivalve as seen in figure 8.

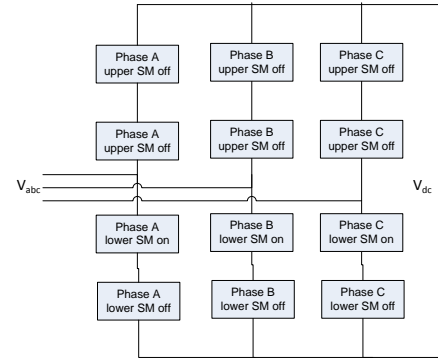


Figure 8: The structure of the simplified passive component model with the 3 phase arms, each of which consists of 2 circuits, one representing the on-state and the other representing the off-state.

As explained earlier the two multivalves in a phase are direct opposite of each other. Therefore, when calculating the component sizes of the upper multivalve, the results can be used for the lower just by switching the number of on and off submodules and vice versa.

### IV. CONTROL

The control used for the MMC is the well-known voltage margin method as described in [9]. The controller will be controlling the active and reactive power and the dc link voltage simultaneously. When controlling the active power, the dc voltage is regulated at the same time. As long as there is power balance between the inverter and the rectifier, the dc voltage will be kept stable. Hence, the current supplied by the rectifier is drawn by the inverter, which means there is no further charging of the dc side. The rectifier though has to transport a bit more active power than the inverter is consuming, since it has to deliver the losses of the HVDC transmission system.

The active power or the dc voltage is controlled by the control of  $\delta$  i.e. the angle between grid and converter voltages. The reactive power is control by the modulation index ( $m$ ).

The apparent power at the point x (see figure 9) can be expressed in terms of the  $dq$  component of the current and voltage as follows.

$$S = \{(V_{xd}i_d + V_{xq}i_q) + j(V_{xq}i_d - V_{xd}i_q)\} \quad (4)$$

$$V_{xq} \approx 0 \quad (5)$$

$$S = \{V_{xd}i_d - jV_{xd}i_q\} \quad (6)$$

Here  $V_{xd}$  and  $V_{xq}$  are the  $dq$  components of the voltage in the point x. While  $i_d$  and  $i_q$  are the  $dq$  components of the current. When assuming that the voltage and current at the ac side are balanced and the  $d$ -axis is aligned to the voltage phasor of phase A in point x,  $V_q$  in point x will be close to zero and negligible. Then equation (6) indicates that the active and reactive powers are proportional to the  $d$  and  $q$  currents respectively. Hence, it is possible to control the active power

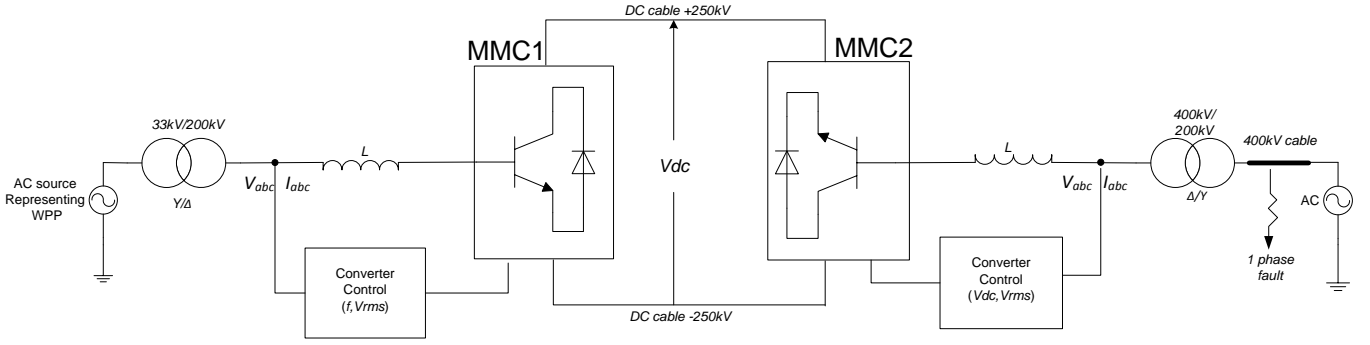


Figure 9: Tested system: WPP connected to a offshore converter station (MMC) and by DC cables to the onshore converter (MMC2).

or the dc voltage by controlling  $i_d$  and the reactive power by  $i_q$ .

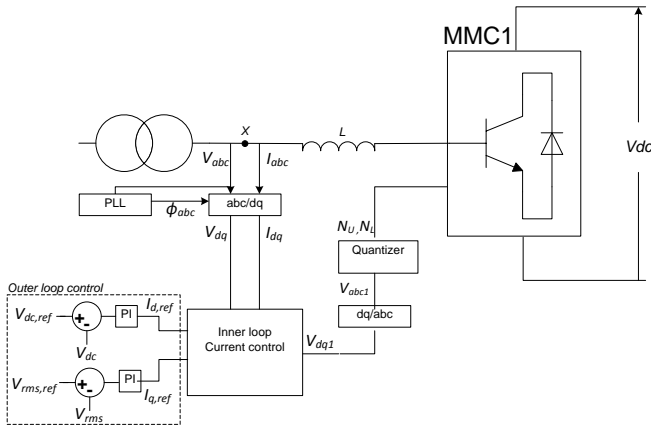


Figure 10: Onshore converter control scheme.  $V_{dc}$  and  $V_{rms}$  used in the outer loop.

The outer loop control provides the current references for the inner loop current control. The offshore converter control differs from figure 10 by the use of frequency instead of  $V_{dc}$  control. The current control then provides the  $dq$  voltage references. Due to the way the converter is modelled we use the method from [10] to get the number of submodules turned on in the upper and lower arm  $N_u$  and  $N_L$  respectively for each phase. These numbers will then be used to calculate the sizes of the parasitic components mentioned earlier.

## V. SIMULATIONS AND CONVERTER OPERATION

In the following are shown results from PSCAD simulations of the system seen in figure 9

The assumed power from the WPP is 600MW. In figure 10 the power is reduced to 80% and increased to 100% after 700ms. In between the dc voltage is decreased to 90% of the  $\pm 300$ kV that the converter is set to start up with. From figure 11a) we find that when the active power is decreased to 80% it is achieved within 100ms. Meanwhile, there is no effect on the dc voltage. Hence, while the control of the rectifier is decreasing, the input power the inverter control is keeping a constant dc voltage without any noticeable changes. From figure 11b) we see that changing the dc voltage happens relatively fast. From 11a) and b) we see that when the dc

voltage is decreased the inverter has to increase its power consumption to discharge the dc voltage to the wanted value. In the meantime the rectifier keeps the power at a constant rate. Figure 11c) shows that since all the changes are done for active power,  $V_q$  is kept almost constant at all times which show the decoupling of the control.

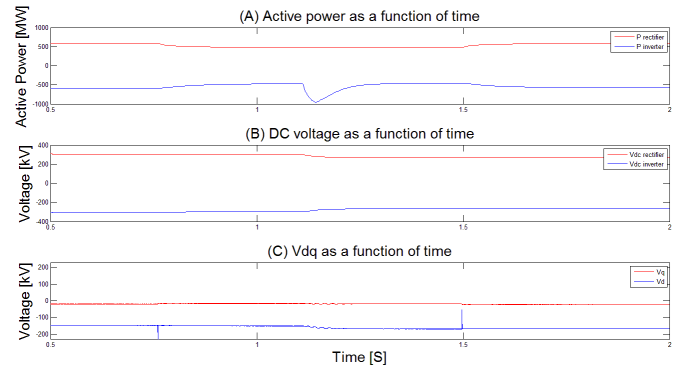


Figure 11: System response for change of control parameters , a) Active power as a function of time, b) dc voltage as function of time, c)  $V_d$  and  $V_q$  as function of time.

As a first example of a transient event, a line-to-ground fault is now applied on a 400 kV transmission line close to the onshore converter. The fault duration is 20ms, it starts at 1s and ends at 1.02s. From figure 12(C) we see that since the fault is very close to the converter it will have a considerable influence on the dc current.

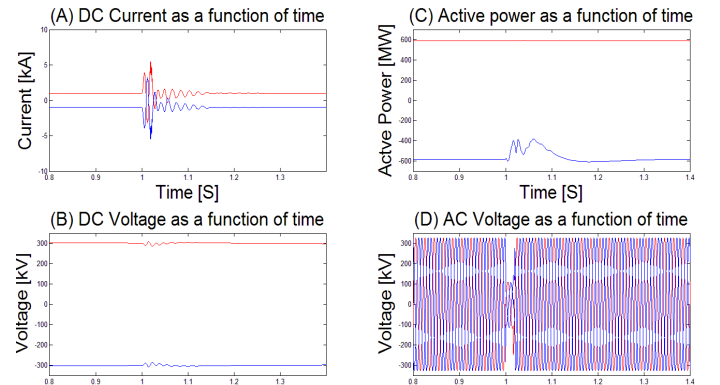


Figure 11: System response during line to ground fault, A) dc current, B) dc voltage, C) Active power, D) onshore AC voltage

While the fault is present, the dc current will show large oscillations, but as soon as it is cleared, the oscillations will become much smaller and get cleared within 100ms from fault clearance. 12(B) shows how the dc voltage control will still try to keep the dc voltage constant, even under fault conditions. Small fluctuations will be present due to the fluctuations in the ac current that is used in the control. The dc power in 12(C) also recovers within 100ms after fault clearance. The ac voltage in 12(D) indicates that the ac voltage control decreases the recovery time.

## VI. CONCLUSION

A typical application of the MMC based HVDC transmission system has been presented. A new method for expressing the MMC converter in terms of passive components has been described. The model gives a simple technique to simulate the entire MMC based HVDC transmission system regardless of the number of levels while keeping the simulation time at an acceptable level. Meanwhile the model integrates all the high frequency aspects and can be implemented in an electro-magnetic transient simulation program. Several time domain and transient simulations have been conducted to demonstrate the behavior of the MMC.

## ACKNOWLEDGEMENTS

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